2. (Amended) The semiconductor device according to claim 1, wherein said plurality of transistors comprise a plurality of MOSFETs formed on a substrate.

3. (Amended) The semiconductor according to claim 2,

wherein said MOSFET includes a core-purpose MOSFET and an I/O-purpose MOSFET, and

wherein said core-purpose MOSFET has a smaller thickness of said gate insulator film than that of said I/O-purpose MOSFET and also has a smaller thickness of said gate electrode than that of said I/O-purpose MOSFET.

Please add the following new claims:

- - 7. (New) The semiconductor device according to claim 1, wherein said plurality of transistors comprise a second lightly doped drain region.

8. (New) The semiconductor device according to claim 7, wherein said first lightly doped drain region is deeper than said second lightly doped drain region.

9. (New) The semiconductor device according to claim 3, wherein said I/O-purpose MOSFET comprises said first lightly doped drain region.

10. (New) The semiconductor device according to claim 3, wherein said core-purpose MOSFET comprises a second lightly doped drain region.

11. (New) The semiconductor device according to claim 2, = clm 3

wherein said MOSFET includes a core-purpose MOSFET and an I/O-purpose MOSFET, and

wherein said core-purpose MOSFET has a smaller thickness of said gate insulator film than that of said I/O-purpose MOSFET. clms 11 & 12 = clm 3

12. (New) The semiconductor device according to claim 2, = Clm 3

wherein said MOSFET includes a core-purpose MOSFET and an I/O-purpose MOSFET, and

wherein said core-purpose MOSFET has a smaller thickness of said gate electrode than that of said I/O-purpose MOSFET.

13. (New) The semiconductor device according to claim 3, wherein said core-purpose MOSFET comprises an N - channel MOSFET for being driven on a supply voltage of about 1.0v.

14. (New) The semiconductor device according to claim 3, wherein said I/O-purpose MOSFET comprises an N - channel MOSFET for being driven on a supply voltage of about 3.3v.

15. (New) The semiconductor device according to claim 1, wherein said first lightly doped drain region comprises an I/O-purpose P-well with an N - type impurity at a predetermined density and a predetermined energy level, said N - type impurity comprises phosphorous.

Cont B2

16. (New) The semiconductor device according to claim 15,

wherein said predetermined density is about $2 \times 10^{13}/cm^2$, and

wherein said predetermined energy level is about 30 keV.

17. (New) The semiconductor device according to claim 1, wherein said second lightly doped drain region comprises a core-purpose P-well with an N - type impurity at a predetermined density and a predetermined energy level, said N - type impurity comprises arsenic.

18. (New) The semiconductor device according to claim 17,

wherein said predetermined density is about $5 \times 10^{14}/cm^2$, and

wherein said predetermined energy level is about 2.5 keV.

19. (New) The semiconductor device according to claim 1,

wherein said plurality of transistors comprise a plurality of sidewalls, said plurality of sidewalls comprising a first sidewall and a second sidewall, and

wherein said first sidewall has a height greater than that of said second sidewall.

20. (New) The semiconductor device according to claim 1, wherein said plurality of transistors comprise said source region and said drain region with an N - type impurity at a predetermined density and a predetermined energy level, said N - type impurity comprises arsenic.

21. (New) The semiconductor device according to claim 20,

wherein said predetermined density is about 5 x 10^{15}/cm^2, and

wherein said predetermined energy level is about 30 keV.

Cont B2

22. (New) A semiconductor device comprising:

a plurality of transistors having different gate insulator film thickness values, said plurality of types of transistors having different thickness values of a gate electrode thereof in correspondence to the thickness values of the gate insulator film thereof,

wherein said plurality of transistors comprise a first lightly doped drain region and a second lightly doped drain region.

23. (New) A semiconductor device comprising:

a plurality of transistors having different gate insulator film thickness values with a polysilicon film layer, said plurality of transistors having different thickness values of a gate electrode thereof in correspondence to the thickness values of the gate insulator film thereof,

wherein said thickness of said gate insulator film varies based on the amount of deposited gate electrode materials.--

REMARKS

Claims 1-3 and 7- 23 are all the claims presently pending in the application. Applicant affirms the election of the invention of claims 1-3. Claims 4-6 have been canceled without prejudice or disclaimer. New claims 7-23 have been added to more particularly define the invention. Claims 1-3 stand rejected on prior art grounds.

Claims 1-3 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Yamane et